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### **Manual versions**

This manual describes the Flasher device. For further information on topics or routines not yet specified, please contact us.

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Manual Version	Revision	Date	Ву	Description
1.00	е	210819	JB	Corrections after review
1.00	d	180109	MF	Update filename information (remove 8.3 filename lim- itation)
1.00	С	180109	MF	Corrected FTP connection picture
1.00	b	180109	MF	Minor changes after review.
1.00	а	171219	MF	Minor changes after review.
1.00	0	171218	MF	Minor changes after review.
0.01	0	171217	MF	Initial version.

## About this document

### Assumptions

This document assumes that you already have a solid knowledge of the following:

- The software tools used for building your application (assembler, linker, C compiler).
- The C programming language.
- The target processor.
- DOS command line.

If you feel that your knowledge of C is not sufficient, we recommend *The C Programming Language* by Kernighan and Richie (ISBN 0--13--1103628), which describes the standard in C programming and, in newer editions, also covers the ANSI C standard.

### How to use this manual

This manual explains all the functions and macros that the product offers. It assumes you have a working knowledge of the C language. Knowledge of assembly programming is not required.

### Typographic conventions for syntax

This manual uses the following typographic conventions:

Style	Used for
Body	Body text.
Keyword	Text that you enter at the command prompt or that appears on the display (that is system functions, file- or pathnames).
Parameter	Parameters in API functions.
Sample	Sample code in program examples.
Sample comment	Comments in program examples.
Reference	Reference to chapters, sections, tables and figures or other doc- uments.
GUIElement	Buttons, dialog boxes, menu names, menu commands.
Emphasis	Very important sections.

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# Chapter 1 Introduction

This documents guides you through the first steps with the Flasher ATE. The goal is to have a first project running with the Flasher ATE. Please take care of the prerequisites listed in chapter *Prerequisites* on page 10.

The Flasher ATE is designed for mass production purpose. If you are familiar with other SEGGER Flasher products and the J-Flash-Tool, migration will be easy.

# Preparing for handshake and remote-controlled mode

#### 2.1 **Prerequisites**

#### 2.1.1 Hardware prerequisites

- The Flasher ATE setup must contain a main board and at least one module board. •
- The Flasher ATE needs to be powered. •
- The target board needs to be connected to the module board. •
- The Flasher ATE needs to be connected to the network. J-Link mode via USB is currently • not supported.



Network connection Target board

#### 2.1.2 Software prerequisites

- You need the J-Flash to generate the Flasher ATE project files and J-Link Configurator • tool. These are available for download at: Flasher Downloads . The tools are included in the Flasher Software and Documentation pack.
- The firmware or a test program for the target device must be available. ٠

### 2.2 Setting up the project files

In order to set up Flasher for the handshake or remote-controlled mode it needs to be configured once using the J-Flash software. For more information about J-Flash, please refer to the *J-Flash Manual* 

After starting J-Flash, create a J-Flash project for the target Flasher, by selecting **File** - > **New Project**.

After the appropriate project has been created, the data file which shall be programmed needs to be loaded, by selecting **File** -> **Open data file**. After this J-Flash should look like in the screen-shot below.

Project - AT91         Image         Mame         Value           Connection         USB [Device 0]         Target interface         JTAG         Mame         Value         Address:         0x100000         x1         x2         x4           Init JTAG speed         200 kHz         Address:         0x100000         x1         x2         x4           Init JTAG speed         12000 kHz         1000000         26         00         00         EF         FF	SEGGER J-Flash ARM V4.58a - [C:\Program Files (x86)\SEGGER\JLinkARM_V458a\Samples\JFlash\ProjectFiles\AT91SAM7X256.jflash]																						
Name         Value           Connection         USB [Device 0]           Target interface         JTAG           Init JTAG speed         200 kHz           JTAG speed         12000 kHz           IAP number         (not used)           IBPre         (not used)           IB00020         06         60         00	<u>File Edit View</u>	<u>Iarget Options W</u>	/indow Help										_				_						 
Name         Value           Connection         USB [Device 0]           Target interface         JTAG           Init JTAG speed         200 kHz           Id00000         7E         FF	Project - ATS	91 🗖 🗖 🖾	Test data	(gene	rated I	oy J-Fla	sh) *																x
Connection         USB [Device 0]         Image interface         Image interface <thimage interface<="" th=""> <thimage interface<="" t<="" td=""><td>Name</td><td>Value</td><td>Address: 0x1</td><td>00000</td><td></td><td>(1 x2</td><td>x4</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></thimage></thimage>	Name	Value	Address: 0x1	00000		(1 x2	x4																
Target interface       JTAG       Hddress       Ø       1       2       3       4       5       6       7       8       9       A       B       C       D       E       F       BSCI1         Init JTAG speed       200 kHz       100000       35       60       60       60       60       94       FE       FF       FF </td <td>Connection</td> <td>USB [Device 0]</td> <td>- ,</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>-</td> <td></td>	Connection	USB [Device 0]	- ,									-											
Init JTAG speed       200 kHz       1000000       2b       00 00 E       FE       FF       FF       FA       FF	Target interface	JTAG	Address	0	1	$\frac{2}{3}$	4	5	6	7	8	9	A DD	B	C	D	E	F	ASC				
Init JTAG speed       200 kHz       100010       FE       FF			100000	- 26	00 0	10 EA	FE	FF	FF	EA	FE	FF	FF	EA	FE	FF	FF	EA				• • • •	
JTAG speed       12000 kHz       100020       00 60 00 10 10 00 00 00 00 00 00 00 00 00 00	Init JTAG speed	200 kHz	100010	FE	FF I	F EH	Юb	90	00	94	FE	FF	FF	EH	FE	FF	FF	EH	-:-	• • • •		;	
TAP number <not used="">       100030       0C       00       &lt;</not>	JTAG speed	12000 kHz	100020	00	60 1	10 E3	10	70	87	EZ	01 0T	60	86	EZ	FD	FF	FF	EH		p			
IRPre       (not used)       100040       10       90       90       90       90       10       90       90       90       90       10       90       90       90       90       10       90       90       90       10       90       90       90       10       90       90       90       10       90       90       90       10       90       90       90       10       90	TAP number	<not used=""></not>	100030	00	00 0	00 00	40	00	00	00	UE	00	90	00	UF 40	00	00	00		• • • •			
MCU       Atmel AT91SAM7X256       14       09       09       09       15       09       09       00       17       09       00       09       17       09       00       09       17       09       00       09       17       09       00       09       17       09       00       09       18       00       00       09       10       00       00       10       00       00       01       10       00       00       10       00       00       01       10       00       00       01       10       00       00       01       10       00       00       11       00       00       01       10       00       00       11       00       00       01       10       00       00       11       00       00       01       10       00       00       11       00       00       01       10       00       00       11       00       00       01       10       00       00       11       00       00       01       10       00       00       12       00       00       02       10       00       00       12       00       00	IRPre	<not used=""></not>	100040	10	00 0	10 00	11	00	00	00	12	00	00	00	13	00	00	00		• • • •			
MCU       Atmel AT915AM7x256       100060       18       09       00       09       19       09       00       09       11       09       00       09       11       09       00       09       11       09       00       09       11       09       00       09       11       09       00       09       11       09       00       01       100       00       01			100050	14	00 0	00 00	15	00	00	00	16	00	00	00	17	00	00	00		• • • •	• • •		
Clock speed       47923200 Hz       100090       10       00	MCU	Atmel AT91SAM7X256	100060	18	00 0	10 00 00 00	19	00	00	00	18	00	90	00	18	00	00	00		• • • •			
Endian         Little         100000         20         00         00         00         21         00         00         00         23         00         00         00         23         00         00         00         23         00         00         00         23         00         00         00         23         00         00         00         23         00         00         00         23         00         00         00         23         00         00         00         23         00         00         23         00         00         23         00         00         23         00         00         00         23         00         00         00         23         00         00         00         23         00         00         00         23         00         00         00         23         00         00         00         23         00         00         00         23         00         00         00         23         00         00         00         23         00         00         00         23         00         00         00         23         00         00         00         00	Clock speed	47923200 Hz	100070	10	00 0	10 00 10 00	10	90	90	99	11	99	90	90	11	99	90	90		••••••			
Check core Id         Yes         100070         24         96         96         96         96         96         96         96         96         96         97         96         96         96         97         96         96         96         97         96         96         96         97         96         96         96         97         96         96         96         97         96         96         96         97         96         96         96         97         96         96         96         97         96         96         96         97         96	Endian	Little	100080	20	00 0	10 00 00 01	21	90	60	99	22	99	99	90	23	99	90	90	·	· · ! ·	"	····#	
Core Id         0x3F0F0F0F         1000H0         28         99         90         90         90         91         91         90         90         91         91         90         91 <td>Check core Id</td> <td>Yes</td> <td>100090</td> <td>24</td> <td>00 0</td> <td>00 00</td> <td>25</td> <td>00</td> <td>00</td> <td>00</td> <td>26</td> <td>00</td> <td>00</td> <td>00</td> <td>27</td> <td>00</td> <td>00</td> <td>00</td> <td>÷</td> <td>·</td> <td>X</td> <td></td> <td></td>	Check core Id	Yes	100090	24	00 0	00 00	25	00	00	00	26	00	00	00	27	00	00	00	÷	·	X		
Use target RAM         Yes         100080         2C         00 <td>Core Id</td> <td>0x3F0F0F0F</td> <td>100000</td> <td>28</td> <td>00 0</td> <td>00 00</td> <td>29</td> <td>90</td> <td>00</td> <td>90</td> <td>ZH</td> <td>00</td> <td>90</td> <td>90</td> <td>28</td> <td>90</td> <td>90</td> <td>00</td> <td>· · ·</td> <td></td> <td>••*</td> <td>+</td> <td></td>	Core Id	0x3F0F0F0F	100000	28	00 0	00 00	29	90	00	90	ZH	00	90	90	28	90	90	00	· · ·		••*	+	
RAM address         0x200000         100000         34         00         00         93         100         00         93         20         00         00         93         90         00         93         20         00         00         93         90         00         93         20         00         00         93         90         00         93         90         00         93         90         00         93         90<	Use target RAM	Yes	100080	20	00 0	00 00	20	90	00	99	ZE	00	99	90	25	99	90	99	<u></u>	•	•••		
RAM size         64 KB         1000100         34         60	RAM address	0x200000	100000	30	00 0	00 00	31	90	00	99	32	00	99	99	33	99	90	90	Ø		••• 4		
Flash memory         AT91SAM7X256 inter         100010         3C         00         3E         00         00         00	RAM size	64 KB	100000	34	00 0	90 00 00 00	35	90	99	99	30	00	99	99	37	99	99	99	4	5.		:	
Flash memory         AT915AM7x256 inter         1000100         30         90         90         90         91         91         90         90         90         91         91         90         90         90         91         91         90         90         90         91         91         90         90         90         91			1000E0	38	00 0	00 00	37	90	00	90	31	00	99	90	38	99	90	90	8			···;	
Manufacturer Afmel 1001100 14 00 00 01 15 00 00 00 12 00 00 01 17 00 00 00	Flash memory	AT91SAM7X256 inter	1000F0	30	00 0	10 00 00 00	30	90	90	99	3E 49	00	99	90	31	99	99	90	<u>``</u>	··- =	•••	· · · · í	
	Manufacturer	Atmel	100100	40	00 0	10 00 10 00	41	90	90	99	42	90	90	99	43	90	90	90	е в	н. г	· · · D		
	Size	256 KB	100110	44	00 0	10 00 10 00	40	90	60	00	40	60	90	90	47	00	00	90	υ	с. т		· · · · G	
	Flash Id	UxU	100120	40	00 0	10 00 10 00	47	00	60	00	10	60	60	00	40	00	60	60	п т				
	Check flash Id	No	100130	- 40 E 0	00 0	10 00 10 00	-1D E 1	00	60	00	10	00	00	00	11	00	00	00	р		P	· · · · e	
	Base address	0x100000	100110	50	00 0	10 00 10 00	51	00	00	00	54	00	00	00	55	00	00	00	T			····o	
Urganization 32 bits x1 chip 100160 58 00 00 59 00 00 00 5A 00 00 00 5B 00 00 0	Urganization	32 bits x 1 chip	100150	58	00 (	00 00	59	00	00	00	50 5A	00	00	00	5B	00	00	00	X	Y.	z	w	
100170         5C         00         00         5D         00         00         5E         00         00         05         F         00         00         00        ]        ]	•	4	100170	5C	00 (	00 00	5D	00	00	00	5E	00	00	00	5F	00	00	00	<u>}-</u> -		··-^	•••-	 •
	LOG																						23
- List of MCU devices read successfully (1964 Devices) Creating new project file [C:\Program Files (x86)\SEGGER\JLinkARM_V458a\Default filash] New project created successfully Close project - Project closed Opening project file [C:\Program Files (x86)\SEGGER\JLinkARM_V458a\Samples\JRlash\ProjectFiles\AT91SAM7X256;flash] Project opened successfully Generating test data 1024 of 1024 sectors selected, 1 range, 0x100000 - 0x13FFFF - Test data generated successfully. (262144 bytes, 1 range) - Completed after 0.261 sec																							
Ready	Ready																						/

Follow the instruction of the J-Flash User Guide to setup your project. You can find further details in chapter 3 "Getting Started" of the J-Flash documentation.

For the Flasher ATE it is required to save the project and the datafile to the hard drive. Therefore select **File** -> **Save Flasher config file** to save the project configuration file and afterwards **File** -> **Save Flasher data file...** to save the project data file.

### 2.2.1 Setting up the network configuration

Before downloading the configuration (project) and program data (data file) to Flasher, the Flasher IP settings need to be configured. This can be done by the J-Link Configurator tool. After starting the JLinkConfig executable the screen should look like this:

SEGGER J-Link Configu	ration V6.22a										
	Emulators connected	via LISB-							Refresh	rate: Norm	• •
		Product		SN	USB Identification	Host Firmware	Emulator Firmware				
										1	
	Emulators connected	via TCP/IP:								Select all	Select none
	# △	Product	Nickname	SN	IP Address	MAC Address	Host Firmware	Emulator Firmware	React.Time C	onnections	
da da gidenda <sup>™</sup> gidenda <sup>™</sup> gidenda <sup>™</sup>	• 0 • 1	Flasher ATE Mainboard Flasher ATE Mainboard		5 871099999	19216811.44 (DHCP) 19216811.187 (DHCP)	00.22:C7:00:00.05 00.22:C7:00:00:68	2017 Nov 20 13:44 2017 Nov 20 13:44	2017 Dec 19 05:40 (New) 2017 Dec 19 03:46 (New)	0.227ms 0.225ms	0 0	
	Log ISEGGER J-Link Con Logging started 8	flagsation U6-22a 2017-12-19 09189								<u>Select all</u>	Select none
								Update firmware	of selected emulator	s	Close
Ready					Searching fo	r emulators: Ready			6 6	emulators fo	und //

Now right-click on your Flasher ATE, choose **Configure** from the context menu and enter your required IP settings in the dialog box that opens up. E.g. like shown in the next picture. Confirm the settings by pressing OK.

	Configure J-Link X	1
lickname	General	ost Fi
	Product Flasher ATE Mainboard V4.00	- )17 N - )17 N
	SN 871099999	
	Nickname FlasherATE Test	
	Max. SW0 speed [kHz] Probe does not support SW0	
	Virtual COM-Port C Enable C Disable The connected debug probe does not support VCOM functionality.	
	IP Configuration	
	IP address 192 . 168 . 11 . 187	
	Gateway 192 . 168 . 11 . 1	
	OK Cancel	
-		-

### 2.2.2 Loading the project to the Flasher ATE

Next we need an FTP client. In the example below we are using the FileZilla FTP client but any other FTP client is fine as well. Create a new connection for the Flasher ATE by choosing **File** -> **Site Manager** and enter the connection data. See the image below. The user name for the FTP connection is admin and the password is 1234.

Site Manager	<u>×</u>
Select Entry:	General Advanced Transfer Settings Charset
FlasherATE	Host: 192.168.11.187 Port:
	Protocol: FTP - File Transfer Protocol
	Encryption: Only use plain FTP (insecure)
	Logon Type: Ask for password
	Background color: None  Comments:
New Site New Eolder	
New Bookmark Rename	
Delete Dupl <u>i</u> cate	
	<u>C</u> onnect <u>O</u> K Cancel

And connect to the Flasher ATE.

### Note

The user name and password is currently only intended for preventing changing the setup by accident. It is not to prevent hackers from accessing the Flasher ATE if it is connected to a network. The password cannot be changed.

#### CHAPTER 2

In the next step the project data needs to be loaded to each of the Flasher ATE modules. Therefore navigate to the project files created by the J-Flash in the section *Setup the project files* on page . The result should look like the next picture.

/z admin@192.168.11.187 - FileZilla	<u>-0×</u>
Ele Edit View Iransfer Server Bookmarks Help	
1 🕢 - 📝 🗇 🔁 🛠 🎋 🍬 🛷 🗉 📯 🖻 🦚	
Host: 192.168.11.187 Username: admin Password: •••• Port: Quickconnect V	
Lost 192. Ibs. 11.15 Username: Jacom Passgori: ●●●● Ert: Quickconnect ● Status: Connecting to 192.158.11.187.21 Status: Connecting to 192.158.11.187.21 Status: Connecting server; it does not support FTP over TLS. Status: Logget does not support ftP over TLS. Status: Logget does not support ftP over TLS. Status: Directory lating of 'f accessful Status: Retrieving directory lating of 'f accessful Status: Retrieving directory lating of 'f MOOLE.OUT' Status: Directory lating of 'f MOOLE.OUT'	×
Local site: C:\FlasherATE\empower\	<b></b>
Implements     Implements       Implements <td></td>	
Filename ^ Filesize Fletype Last modified Filename ^ Filesize Filetype Last modified	Permissions Owner/Group
Image: CFG         3,672         PEX File         17-12-08 14:13:07         Image: FLASHER         File folder         80.01-01           Image: PLASHER.CFG         4,096         CFG File         17-12-14 11:44:37         Image: FLASHER.CFG         4,096         CFG File         80.01-01           Image: PLASHER.DAT         2,115,584         DAT File         17-12-14 11:44:58         Image: FLASHER.DAT         133,120         DAT File         80.01-01           Image: PLASHER.NIT         64         Configuration s         17-12-14 11:44:40         Image: FLASHER.INI         64         Configurati         80.01-01           Image: PLASHER.NI         642         LOG File         17-12-14 11:44:40         Image: SERIAL.TXT         2         TXT File         80.01-01	drw-rr root root -rw-r root root -rw-r root root -rw-r root root -rw-r root root
5 files. Total size: 2,124,078 bytes 4 files and 1 directory. Total size: 137,282 bytes	
Server/Local file     Direction     Remote file     Size     Priority     Status       admin@192.168.11.137     C:\Users\WichaelF\Desktop\    >     /MODULE.003/stm32f030.cfg     4,096     Normal       C:\Users\WichaelF\Desktop\    >     /MODULE.003/stm32f030.dat     133,120     Normal	
Queued files (2) Failed transfers Successful transfers	🖉 🖼 Queue: 134.0 KiB

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Next upload the files to the modules. Select the module.xyz folder in the remote site view. Then select the files:

- flasher.cfg and
- flasher.dat.

Choose **Upload** from the context menu to upload them to the module folder.

	·····				
Filename 🔺		File	esize	Filetype	Last modi
C:\Use	FG AT Upload Add files to queue Open Edit Create directory Create directory an Refresh	3 4 2,115 d enter it	,672 ,096 ,584 64 662 Ren /MC	PEX File CFG File DAT File Configuration s LOG File note file DULE.003/stm32f03	17-12-08 17-12-14 17-12-14 17-12-18 17-12-14 30.cfg 30.cfg
Queued file:	Delete Rename	Fers Suc	cessfi	ul transfers	

### Note

This step needs to be repeated for every connected module.

If your device needs one or more script files (file extension .pex) you must upload them to the sub-folder **ProjectName** in the module's folder. The sub-folder has to be named the same as the config file. So in our example case it is "Flasher"

Now everything is prepared for programming the targets.

# **Programming the targets**

### 3.1 Overview

There are 3 ways to control Flasher ATE operation:

- Terminal communication via Telnet.
- Terminal communication via RS232.
- Via Handshake lines: 3 lines on the serial interface are used:
  - 1 line is an input and can be used to start operation,
  - 2 lines are outputs and serve as busy and status signals.

### 3.1.1 Starting the programming sequence via telnet protocol

A client application can connect to the Flasher ATE via Telnet on port 23. Find below a screen-shot of the Flasher which is remote controlled via Telnet using the TeraTerm terminal tool.



You can check if the Flasher ATE is ready to accept commands using the command <code>#status</code>. If yes the answer is <code>#STATUS:READY</code>.

First, the project file that shall be flashed. Use the command: #select [modulenumber] [project file name], e.g. #select 1 FLASHER. Repeat the step for every module.

### Note

The file extensions are added by the firmware.

Second, select the module(s) which shall be used for programming, using the command: #selmodule [1st modulenumber], [2nd modulenumber]..., e.g. #selmodule 1,2.

Third, start the programming with the command #auto \*.

The picture shows the terminal after executing the commands.

🔟 192.168.11.187 - Tera Term VT	
<u>File Edit Setup Control Window Help</u>	
J-Link / Flasher ATE Mainboard V1 telnet-shell. J-Link / Flasher ATE Mainboard V1 conpiled Dec 19 2017 09:46:04 #select 1 FLASHER #HCK #Select 2 FLASHER #ACK #OK #Select 2 FLASHER #ACK #ACK #SelectED:1,2 #auto * #ACK #ACK #ESULT:1:#OK (Total 3.732s, Erase 0,544s, Prog 1.788s, Verify 0.246s) #RESULT:2:#OK (Total 3.732s, Erase 0,544s, Prog 1.788s, Verify 0.246s) #DONE	

### 3.1.2 Starting the programming sequence via RS232

To use the RS232 connection for remote control of the Flasher ATE open a terminal tool, e.g. TeraTerm, and open the serial connection to the Flasher ATE. The serial port settings are:

- baud rate 9600 bits/s,
- data bits 8,
- parity none and
- stop bits 1.



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You can check if the Flasher ATE is ready to accept commands using the command #status. If yes the answer is #STATUS:READY.

First, choose the project file that shall be flashed. Use the command: #select [modulenumber] [project file name], e.g. #select 1 FLASHER. Repeat the step for every module.

### Note

The file extensions are added by the firmware.

Second, select the module(s) which shall be used for programming, using the command: #selmodule [1st modulenumber], [2nd modulenumber]..., e.g. #selmodule 1,2.

Third, start the programming with the command #auto \*.

The picture shows the terminal after executing the commands.



### 3.1.3 Starting the programming sequence via handshake protocol

The Flasher can be remote-controlled by automated testers without the need of a connection to a PC. Therefore the Flasher is equipped with additional hardware control functions, which are connected to the SUBD9 male connector, normally used as RS232 interface to the PC.

The following diagrams show the internal remote control circuitry of Flasher:





Pin No.	Function	Description
1	START	A positive pulse of any voltage between 5 and 30V with duration of min. 30 ms starts "Auto" function (Clear / Program / Verify) on falling edge of pulse. The behavior of the "Auto" function depends on the project settings, chosen in J-Flash at the <b>Production</b> tab.
4	BUSY	As soon as the "Auto" function is started, BUSY becomes active, which means that transistor is switched OFF.
5	GND	Common Signal ground.
7	ОК	This output reflects result of last action. It is valid after BUSY turned back to passive state. The output transistor is switched ON to reflect OK state.

### Note

As the Flasher ATE is a modular system, using the handshake remote control START always triggers the "Auto" function of every connected module. The BUSY line is signaled as long as any module is still busy and the OK line only reports "OK" in case

every module has successfully completed the operation. We recommend using the ASCII command interface, described in the next chapter, for the Flasher ATE as it provides better remote control capabilities.

# **Additional Information**

- Flasher ATE documentation: The full documentation of the Flasher ATE (including the ASCII command protocol) is available here: *Flasher ATE User Guide*
- Flasher ATE web page: Additional information can also be found on our web page *Flasher* ATE Website
- J-Flash-Tool: The J-Flash-Tool is a GUI based tool to create project files for the SEGGER Flashers.

# Glossary

### Flasher ATE

Flasher ATE is the SEGGER production programmer for automated test equipment.

#### **ASCII command protocol**

ASCII command protocol is a ASCII character based protocol to control the Flasher ATE actions.

### J-Flash

*J-Flash* is a tool to create project files for the SEGGER Flasher products.

### J-Link-Config

*J-Link-Config* is a Configuration-Tool for SEGGER Flashers and J-Links.

#### Telnet

*Telnet* is a TCP-based network protocol to transfer characters between two end points.

#### RS232

*RS232* is a hardware standard for asynchronous data transfer between two end points.